

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 14069-003001	Application No. 10/030,639
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Jochen Friedrich Kuhmann et al.	
		Filing Date January 2, 2002	Group Art Unit 2874

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
<i>JD</i>	AA	5,907,646	May 25, 1999	Kitamura			
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents or Published Foreign Patent Applications								
Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AQ	
	AR	
	AS	
	AT	

Examiner Signature <i>[Signature]</i>	Date Considered 5/28/04
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

FORM HDP-1449 (Based on Form PTO-1449) PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE CITATION (Use several sheets if necessary) Sheet 1 of 1	ATTORNEY DOCKET No.	SERIAL No.
	45900-000716	10/030,639
	APPLICANT	
	Jochen F. Kuhmann, et al.	
	FILING DATE	GROUP
January 2, 2002	Unknown	

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Ref. Desig.	Examiner's Initials	Document Number	Date	Name	Class/ Subclass	(If appropriate) Filing Date
DS	DS	4,356,047	10/26/1982	Gordon et al.		7
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		EP0807838A1	11/19/1997	European Patent Application			
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	DS	S.A. Meritt, et al., "A Rapid Flip Chip Die Bonding Method for Semiconductor Laser Diode Arrays", 1997, pages 775-779.
	DS	J. Gates, et al., "Hybrid Integrated Silicon Optical Bench Planar Lightguide Circuits", 1998, total of 9 pages.
	DS	Hans L. Althaus, et al., "Microsystems and Waferprocesses for Volume Production of Highly Reliable Fiber Optic Components for Telecom-and Datacom-Application, 1997, pages 7-15.
	DS	Masataka ITO, et al., "Use of AuSn Solder Bumps in Three-dimensional Passive Aligned Packaging of LD/PD Arrays on Si Optical Benches, 1996, pages 1-7.

Examiner:

Date Considered:

5/28/04

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